University of Dayton

ECE

Mumma Radar Lab

Comprehensive VHDL

Fall 2016

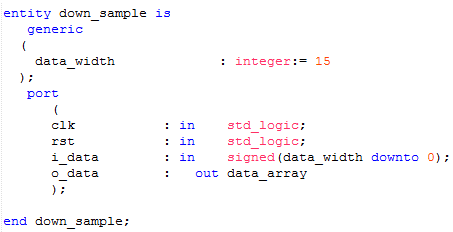
Homework 7

Down Sampling

In this homework, you will be designing a Down Sampling block in VHDL.

You will be given data in text file (data.text), you need to down-sampling this data by 2, 4, and 8.

Please use Package (for data\_array) and Genetic (for data\_width) to configure the following design entity:



Please save the three out down\_sampling data in separate files and then plot the three data.

You should get plots like:

